1-28-03

Attorney Docket No.: 015685.P096 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)
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Orchard)
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Application No: 09/823,928)
)
Filed: March 31, 2001)
)
For: AN ARCHITECTURE AND RELATED)
METHODS FOR EFFICIENTLY)
PERFORMING COMPLEX ARITHMETIC)

Examiner: Not Yet Assigned

Art Unit: 2122

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination of the above-referenced U.S. Patent Application, please enter this amendment.

IN THE SPECIFICATION

Please replace the paragraph beginning on page 9, line 4 with the following:

Fig. 3 illustrates a block diagram of an example extensible, hyperpipelined summing module architecture 304, in accordance with one example embodiment of the present invention. As introduced above, the innovative architecture of summing module 304 is dynamically implemented within one or more CLB (202) blocks of an FPGA by an instance of summing module generator 222. In accordance with the illustrated example implementation of Fig. 3, summing module 304 is depicted comprising a dynamically generated, pipelined hybrid Wallace adder tree 306 of one or more stages (extensible to a hyperpipelined Wallace tree, i.e., 306A-N) which feeds a final, m-input adder stage 318. For example, the final m-input adder stage 318 may be a stage of two-input adders adder stage 318. As shown, the hybrid Wallace tree 306A-N is presented comprising a dynamically determined number of full-adders (fa) and associated registers (R) 308, half-adders (ha) and associated registers (R) 310 and registers (R) 312. Those skilled in the art will appreciate that each of the hybrid elements are readily implemented within